AiP5916
16-key Touch Chip

Product Specification

Specification Revision History：

Version	Date	Description
2018-12-A1	2018-12	New
2023-02-B1	2023-02	Update the template
2025-03-B2	2025-03	Modify the content

Contents

1、General Description

AiP5916 is a capacitive touch key circuit that provides up to 16 touch key channels. Sensitivity can be adjusted via external capacitors and command configurations. Each key channel can be independently enabled/disabled, and disabled channels can be configured as general-purpose I/O for MCU I/O expansion. AiP5916 features a built-in I^2C interface for direct controller connectivity.

Features:

- 16 independent touch key channels
  Configurable as single-key mode or multi-key mode
  Individual channel enable/disable control
  Disabled channels configurable as general-purpose I/O
- Adjustable sensitivity:
  Hardware adjustment via external capacitor on C0 pin
  Software-adjustable globally or per-key
  Compatible with various capacitive touch key designs
  Supports panel thickness≤15mm
- Automatic adaptation to ambient temperature/humidity variations
- Communication interface: I^2C interface
  Includes key-status indicator output (usable as MCU interrupt signal)
- Low power consumption:
  1MHz operation: 70μA@5V (typ.)
  500kHz operation: 43μA@5V (typ.)
  250kHz operation: 30μA@5V (typ.)
  125kHz operation: 23μA@5V (typ.)
  Config-mode quiescent current: 1μA@5V
- Package information: QFN24, SSOP24

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed reel quantity	Notes
AiP5916QB24.TB	QFN24	AiP5916	490 PCS/plate	10 plate/box	4900 PCS/box	Dimensions of plastic enclosure: 4.0mm×4.0mm Pin spacing: 0.50mm
AiP5916VB24.TB	SSOP24	AiP5916	50 PCS/tube	200 plate/box	10000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 0.635mm

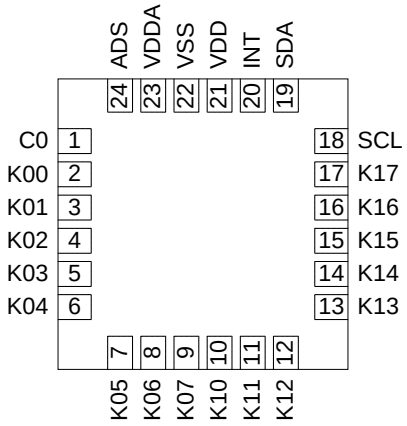
Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP5916QB24.TR	QFN24	AiP5916	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 4.0mm×4.0mm Pin spacing: 0.50mm
AiP5916VB24.TR	SSOP24	AiP5916	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 0.635mm

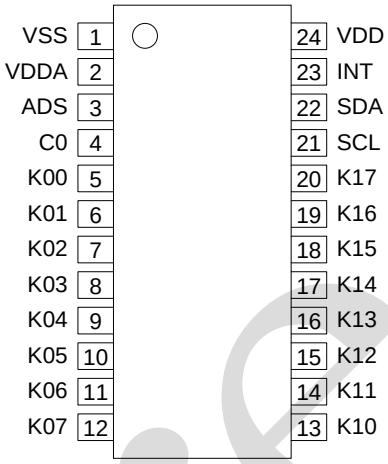
Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram



QFN24



SSOP24

2.2、Pin Description

2.2.1、QFN24 Pin Description

Pin No.	Symbol	I/O	Description
1	C0	I/O	external capacitance
2	K00	I/O	key port/general-purpose IO port
3	K01	I/O	key port/general-purpose IO port
4	K02	I/O	key port/general-purpose IO port
5	K03	I/O	key port/general-purpose IO port
6	K04	I/O	key port/general-purpose IO port
7	K05	I/O	key port/general-purpose IO port
8	K06	I/O	key port/general-purpose IO port
9	K07	I/O	key port/general-purpose IO port
10	K10	I/O	key port/general-purpose IO port
11	K11	I/O	key port/general-purpose IO port
12	K12	I/O	key port/general-purpose IO port
13	K13	I/O	key port/general-purpose IO port
14	K14	I/O	key port/general-purpose IO port
15	K15	I/O	key port/general-purpose IO port
16	K16	I/O	key port/general-purpose IO port
17	K17	I/O	key port/general-purpose IO port
18	SCL	I	I2C communication CLK input port
19	SDA	I/O	I2C communication CLK input port
20	INT	O	key status indicator port
21	VDD	POWER	power
22	VSS	POWER	ground
23	VDDA	I	connected to VDD or left floating
24	ADS	I	I2C slave address selection

2.2.2、SSOP24 Pin Description

Pin No.	Symbol	I/O	Description
1	VSS	POWER	ground
2	VDDA	I	connected to VDD or left floating
3	ADS	I	I2C slave address selection
4	C0	I/O	external capacitance port
5	K00	I/O	key port group 0/general-purpose IO port
6	K01	I/O	key port group 0/general-purpose IO port
7	K02	I/O	key port group 0/general-purpose IO port
8	K03	I/O	key port group 0/general-purpose IO port
9	K04	I/O	key port group 0/general-purpose IO port
10	K05	I/O	key port group 0/general-purpose IO port
11	K06	I/O	key port group 0/general-purpose IO port
12	K07	I/O	key port group 0/general-purpose IO port
13	K10	I/O	key port group 1/general-purpose IO port
14	K11	I/O	key port group 1/general-purpose IO port
15	K12	I/O	key port group 1/general-purpose IO port
16	K13	I/O	key port group 1/general-purpose IO port
17	K14	I/O	key port group 1/general-purpose IO port
18	K15	I/O	key port group 1/general-purpose IO port
19	K16	I/O	key port group 1/general-purpose IO port
20	K17	I/O	key port group 1/general-purpose IO port
21	SCL	I	I2C communication CLK input port
22	SDA	I/O	I2C communication data port
23	INT	O	key status indicator port
24	VDD	POWER	power

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, unless otherwise specified)

Parameter	Symbol	Conditions	Rated value	Unit
supply voltage	VDD	-	-0.3 to +6.5	V
input voltage	V_I	all ports	-0.3 to VDD+0.3	V
output voltage	V_O	all ports	-0.3 to VDD+0.3	V
high level output current	I_{OH}	INT, Kx	-10	mA
low level output voltage	I_{OL}	INT, Kx	20	mA
storage temperature	T_{stg}	-	-65 to +150	℃
soldering temperature	T_L	10s	260	℃

3.2、Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
supply voltage	VDD	2.2	5.0	5.5	V
I2C input high level	V_{IH}	0.8VDD	-	-	V
I2C input low level	V_{IL}	-	-	0.2VDD	V
ambient temperature	T_{amb}	0	-	+70	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics

(T_{amb}=25℃, VDD=5V, VSS=0V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	VDD	-	2.2	5	5.5	V
input high level	V_{IH}	VDD=2.2V to 5.5V, SCL, SDA, ADS	0.8VDD	-	VDD	V
		VDD=2.2V to 5.5V, Kx	VDD-0.1	-	VDD	V
input low level	V_{IL}	VDD=2.2V to 5.5V, SCL, SDA, ADS	0	-	0.2VDD	V
		VDD=2.2V to 5.5V, Kx	0	-	0.1	V
output high level	V_{OH}	VDD=2.2V to 5.5V, I_{OH}=-10mA, INT, Kx	VDD-1.0	-	-	V
output low level	V_{OL}	VDD=2.2V to 5.5V, I_{OL}=20mA, SDA, INT, Kx	-	-	1.0	V
input high level leakage current	I_{IH}	SCL, SDA, ADS	-	-	1	μA
input low level leakage	I_{IL}	SCL, SDA	110	140	170	μA
		ADS	-	-	1	μA
pull-up resistor	R_{PU}	VDD=5V, SCL, SDA	-	35	-	KΩ
		VDD=3V, SCL, SDA	-	70	-	KΩ
supply current	I_{STB}	sleep mode	-	0.7	2	μA
operating current	I_{DD}	Active mode, 1MHz CLK	-	70	90	μA
		Active mode, 500KHz CLK	-	43	60	μA
		Active mode, 250KHz CLK	-	30	50	μA
		Active mode, 125KHz CLK	-	23	40	μA

3.3.2、AC Characteristics

(T_{amb}=25℃, VDD=5V, VSS=0V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
input capacitance	C_{IN}	-	-	-	10	pF
output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

4、Function Description

4.1、Function Registers List

No.	Function Register	Address	Description
1	system control register	0x3A	enable key detection/configuration mode
2	active mode register	0x21	configure the system operating mode
3	baseline update configuration register	0x22	configure the internal detection reference update speed
4	development mode register 1	0x2D	turn on/off the development mode
5	development mode register 2	0x2A	turn on/off the development mode
6	key channel enable control register 0	0x23	turn on/off the key port
7	key channel enable control 1	0x24	turn on/off the key port
8	IO function configuration register 0	0x18	configure the general purpose input/output
9	IO function configuration register 1	0x19	configure the general purpose input/output
10	IO output data register	0x1A	configure the general purpose output state when general purpose is set as output mode
11	IO output data register 0	0x1B	configure the general purpose output state when general purpose is set as output mode
12	IO input data register (R)	0x1C	configure the general purpose input state when general purpose is set as input mode (read only)
13	IO input data register (R)	0x1D	configure the general purpose input state when general purpose is set as input mode (read only)
14	global sensitivity register	0x20	configure the global key sensitivity
15	key threshold register 0	0x00~0x07	configure a single key sensitivity
16	key threshold register 1	0x08~0x0F	configure a single key sensitivity
17	key value register (R)	0x34	store the current key detection results (read only)
18	key value register (R)	0x35	store the current key detection results (read only)

4.2、Register Description

4.2.1、System Control Register (Address 0x3A)

Bit	B7	B6	B5	B4	B3	B2	B1	B0	Reset value
Address 0x3A	SYS								0x00

SYS= 0x5A Enter the configuration mode, the touch detection function is off, and the function register can be set

SYS= 0x00 Enter the active mode while initializing the touch detection module

After the circuit is powered on, although SYS=0x00, the circuit does not stably perform the touch function because the touch detection module is not internally initialized. Therefore, after the power-on, must first enter the configuration mode, and then enter the operating mode.

4.2.2、Operating Mode Register (Address 0x21)

Bit	B7	B6	B5	B4	B3	B2	B1	B0	Reset value
Address 0x21	0	IO	KT	0	INT	M/S	OSC		0x00

IO= 0 turn off the channel of key function, and can be used as the detection result output of another set of corresponding keys

IO= 1 turn off the channel of key function, and can be used as the general purpose IO (KT must be set as 1)

The corresponding relationship between key and detection output port when IO bit is set as 0:

Key	K00	K01	K02	K03	K04	K05	K06	K07	K10	K11	K12	K13	K14	K15	K16	K17
Detection result output	K17	K16	K15	K14	K13	K12	K11	K10	K07	K06	K05	K04	K03	K02	K01	K00

KT= 0 When IO=0, turn off the channel of function key and enable pass through mode for output

KT= 1 When IO=0, turn off the channel of key function and enable inversion mode for output

Output mode	Description
Pass through mode	When a key is pressed, the detection result output port asserts LOW When the key is released, the detection result output port asserts HIGH
Inversion mode	A key press triggers a single toggle of the output level on the detection result port Key release leaves the output state of the detection port unchanged from its previous state At startup, the initial output state defaults to HIGH-level

INT= 0 When a key is pressed, the INT port outputs "L"; when released, it returns to "H"

INT= 1 When a key is pressed, INT port outputs fixed-duration low pulse

M/S= 0 Single-key mode, the circuit can recognize only one press at a time

M/S= 1 Multi-key mode, the circuit can recognize multiple simultaneous key presses

OSC= 00 System clock selection 1000KHz

OSC= 01 System clock selection 500KHz

OSC= 10 System clock selection 250KHz

OSC= 11 System clock selection 125KHz

B7, B4 must be set to 0, otherwise the circuit will fail to operate properly

In single key mode when multiple keys are pressed simultaneously:

If pressed sequentially, only the first pressed key is detected.

If pressed at the same instant, all key presses are discarded.

Higher system clock speeds increase power consumption but improves key detection efficiency.

4.2.3、Detection Reference Update Register (Address 0x22)

Bit	B7	B6	B5	B4	B3	B2	B1	B0	Reset value
Address 0x22	UD								0x20

UD= 0x20 Update key detection baseline in default time

UD= 0x00 Update key detection baseline in high-speed mode

High-speed mode accelerates the baseline auto-upgrading but degrades circuit noise immunity. Thus, modifying this register configuration is strongly not recommended unless under unavoidable scenarios, including:

1、Unavoidable power-on with pre-pressed keys

2、Unavoidable rapid post-power-on temperature/humidity fluctuations

3、Other sudden and drastic environmental/hardware variations

4.2.4、Development Mode Register 1/2 (Address 0x2D, 0x2A)

Bit	B7	B6	B5	B4	B3	B2	B1	B0	Reset value
Address 0x2D	TM0								0x00
Address 0x2A	TM1								0x10

TM0= 0x00
TM1= 0x10
Normal operating mode

TM0= 0x80
TM1= 0xFF
Development mode, relax the key detection standard to allow triggering key functions through direct physical contact with key pads, spring, and key pins of the chip.
The settings of the "key threshold control register" become ineffective in this state. Therefore, modifying this register is discouraged during normal operation.

4.2.5、Key Channel Enable Control Register0/1 (Address 0x23, 0x24)

Bit	B7	B6	B5	B4	B3	B2	B1	B0	Reset value
Address 0x23	K07	K06	K05	K04	K03	K02	K01	K00	0x00
Address 0x24	K17	K16	K15	K14	K13	K12	K11	K10	0x00

K0n，K1n= 0 Turn on the corresponding K0n, K1n ports

K0n，K1n= 1 Turn off the corresponding K0n, K1n ports

4.2.6、IO Function Configuration Register 0/1 (Address 0x18, 0x19)

Bit	B7	B6	B5	B4	B3	B2	B1	B0	Reset value
Address 0x18	IO07	IO06	IO05	IO04	IO03	IO02	IO01	IO00	0x00
Address 0x19	IO17	IO16	IO15	IO14	IO13	IO12	IO11	IO10	0x00

IO0n，IO1n= 0 When key functions are disabled for K0n, K1n ports, the pins are used as IO outputs

IO0n，IO1n= 1 When key functions are disabled for K0n, K1n ports, the pins are used as IO inputs

The function is active only when both IO and KT bits in the operating mode register are set to 1
All channels feature built-in pull-up resistors when configured as general-purpose IO

4.2.7、IO Output Data Register 1/0 (Address 0x1A, 0x1B)

Bit	B7	B6	B5	B4	B3	B2	B1	B0	Reset value
Address 0x1A	O17	O16	O15	O14	O13	O12	O11	O10	0xFF
Address 0x1B	O07	O06	O05	O04	O03	O02	O01	O00	0xFF

O0n，O1n= 0 Output "L" when K0n and K1n ports are configured as output IOs

O0n，O1n= 1 Output "H" when K0n and K1n ports are configured as output IOs

4.2.8、IO Input Data Register 0/1（Read only, address 0x1C, 0x1D）

Bit	B7	B6	B5	B4	B3	B2	B1	B0	Reset value
Address 0x1C	I07	I06	I05	I04	I03	I02	I01	I00	0x00
Address 0x1D	I17	I16	I15	I14	I13	I12	I11	I10	0x00

I0n，I1n= 0 The external pin state is "L" when K0n, K1n are configured as input IOs

I0n，I1n= 1 The external pin state is "H" when K0n, K1n are configured as input IOs

4.2.9、Global Sensitivity Register (Address 0x20)

Bit	B7	B6	B5	B4	B3	B2	B1	B0	Reset value
Address 0x20	GSR								0x02

GSR= 0x01~0x0F Adjust the sensitivity of all the key ports

A smaller configuration value reduces detection sensitivity, shortens scan cycle time, and supports faster key press input

A larger configuration value increases detection sensitivity, extends scan cycle time, and requires slower key press frequency

4.2.10、Key Threshold Control Register 0/1 (Address 0x00~0x0F)

Bit	B7	B6	B5	B4	B3	B2	B1	B0	Reset value
Address 0x00	OR00								0x04
Address 0x01	OR01								0x04
Address 0x02	OR02								0x04
Address 0x03	OR03								0x04
Address 0x04	OR04								0x04
Address 0x05	OR05								0x04
Address 0x06	OR06								0x04
Address 0x07	OR07								0x04
Address 0x08	OR10								0x04
Address 0x09	OR11								0x04
Address 0x0A	OR12								0x04
Address 0x0B	OR13								0x04
Address 0x0C	OR14								0x04
Address 0x0D	OR15								0x04
Address 0x0E	OR16								0x04
Address 0x0F	OR17								0x04

OR0n=	0x01~0xFF	OR0n/OR1n respectively correspond to keys K0n/K1n
OR1n=	0x01~0xFF	Used to individually configure the sensitivity of a specific key. Lower setting values indicate higher sensitivity.

4.2.11、Key Value Register 0/1（Read only, address 0x34, 0x35）

Bit	B7	B6	B5	B4	B3	B2	B1	B0	Reset value
Address 0x34	VR07	VR06	VR05	VR04	VR03	VR02	VR01	VR00	0x00
Address 0x35	VR17	VR16	VR15	VR14	VR13	VR12	VR11	VR10	0x00

The register can only perform read operations. VRn/VR1n corresponds to keys K0n/K1n respectively, which are used to store the state of each key.

VR0n，VR1n=	0	Key K0n/K1n is not currently pressed
VR0n，VR1n=	1	Key K0n/K1n is currently pressed

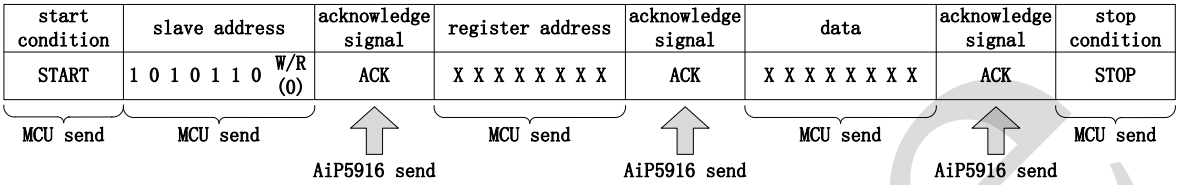
4.3、I²C Communication Method Description

4.3.1、Overview

AiP5916 provides standard I²C interface. Serial data line (SDA) and serial clock line (SCL) have built-in pull-up resistance. The SDA and SCL must remain HIGH-level when the bus is idle.

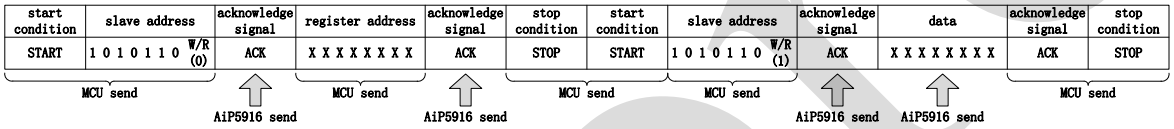
AiP5916 can only operate as an I²C slave device. The slave address is configurable via the ADS pin state. Address 1010110 when ADS is floating or pulled high; address 1010111 when ADS is pulled low.

AiP5916 utilizes an "address + data" protocol for I²C communication operations:



Write operation

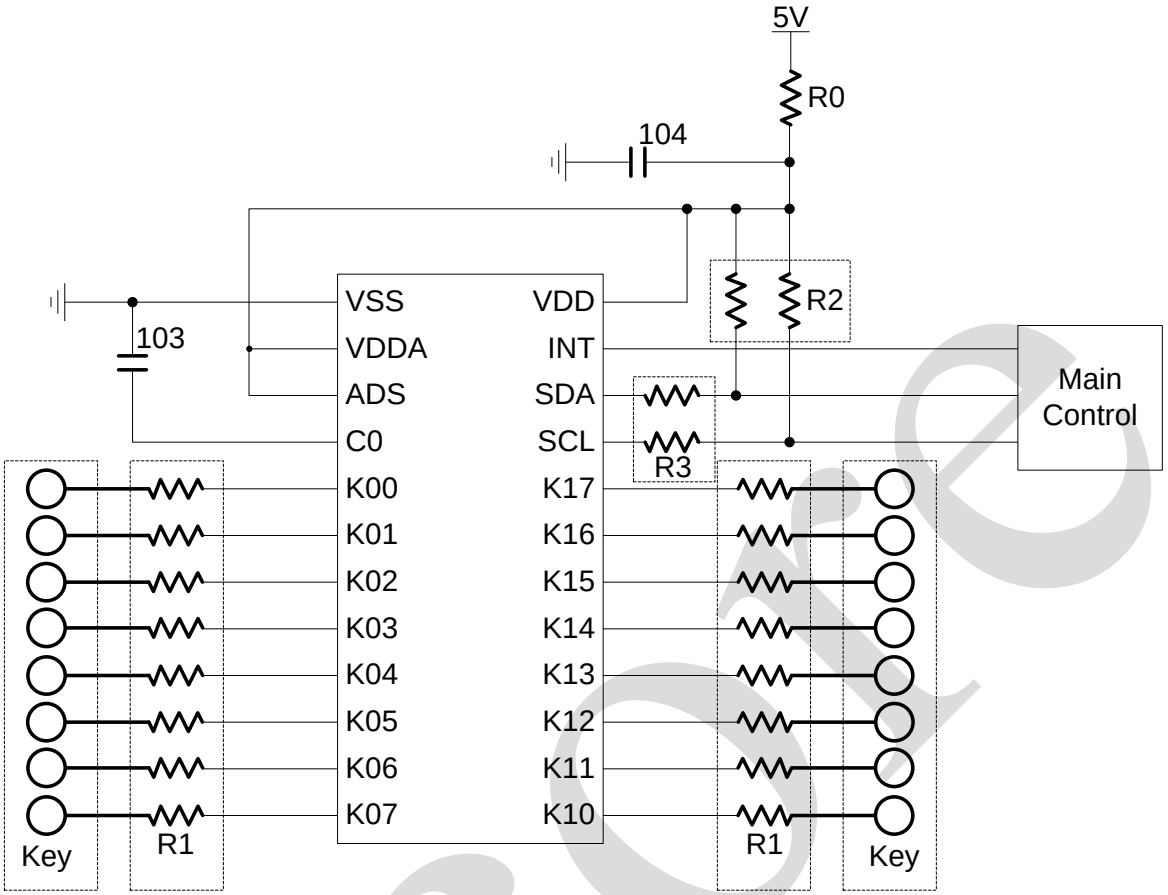
Following the slave address, the W/R bit indicates the read/write operation direction. When W/R=0, a write operation is performed subsequently When W/R=1, a read operation is performed subsequently.



Read operation

For read operations, a complete START-STOP transaction cycle is required to set the target register address, followed by a subsequent START-STOP cycle to read the data.

5、Typical Application Circuit And Application Note



*R0 resistor + 104 capacitor enhance power rail stability and suppress high-frequency noise. Recommended: R0=22Ω

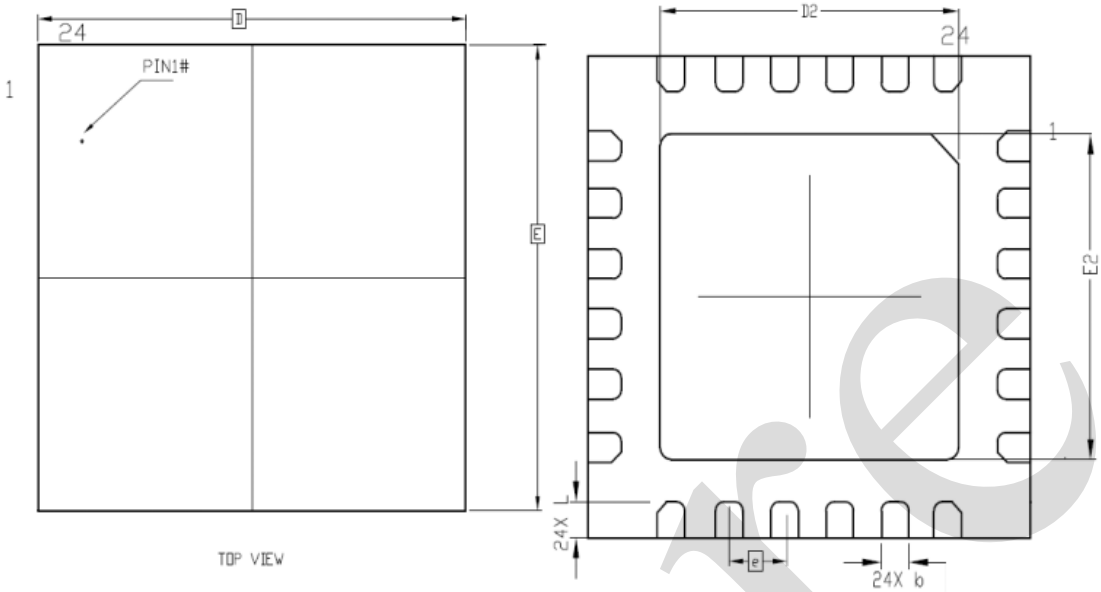
*Series resistor R1 debounces mechanical contacts and filters EMI. Recommended range: 1K～20KΩ

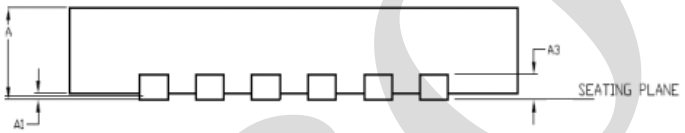
*SDA, SCL ports pull-up R2, recommended range: 5K～10KΩ

*SDA, SCL ports pull-up R2, recommended range: 200～2000Ω

6、Package Information

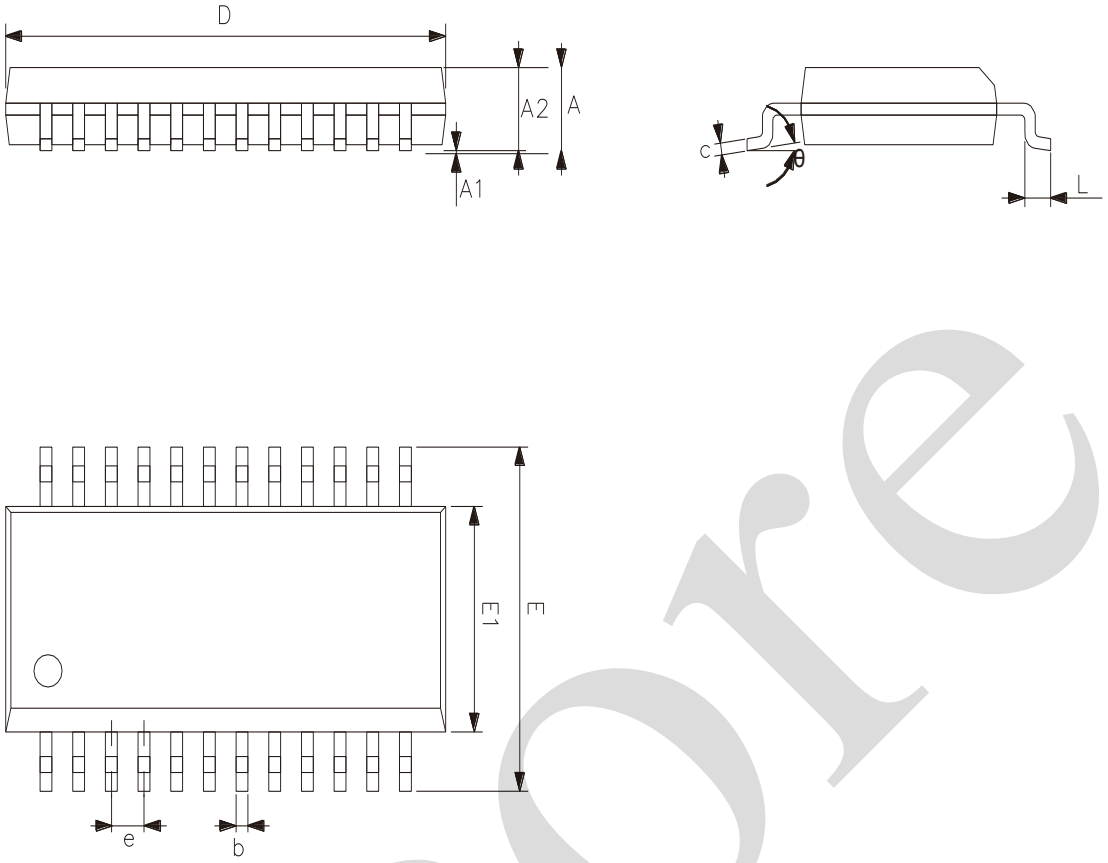
6.1、QFN24





2024/01/B	Dimensions In Millimeters	
Symbol	Min	Max
A	0.70	0.80
A1	0	0.05
A3	0.20	
b	0.20	0.30
D	3.90	4.10
E	3.90	4.10
D2	2.60	2.80
E2	2.60	2.80
e	0.50	
L	0.25	0.45

6.2、SSOP24 (0.635mm)



2023/12/A	Dimensions In Millimeters	
Symbol	**Min**	**Max**
A	1.35	1.75
A1	0.10	0.25
A2	1.30	1.55
b	0.23	0.47
c	0.19	0.26
D	8.45	8.85
E	5.80	6.20
E1	3.70	4.10
e	0.635	
L	0.40	0.80
θ	0°	8°

7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notes

We recommend you to read this chapter carefully before using this product.

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