AiP74HC589

8-Bit Serial or Parallel-Input/Serial-Output Shift Register with 3-State Output

Product Specification

Specification Revision History：

Version	Date	Description
2023-08-A1	2023-08	New

Contents

1、General Description

The AiP74HC589 device consists of an 8−bit storage latch which feeds parallel data to an 8−bit shift register.Inputs include clamp diodes. It enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Features:

- Supply voltage range from 2.0 to 6.0 V
- Specified from -40℃ to +125℃
- Packaging information: DIP16/SOP16/TSSOP16

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74HC589 DA16.TB	DIP16	74HC589	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
AiP74HC589 SA16.TB	SOP16	74HC589	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
AiP74HC589 TA16.TB	TSSOP16	74HC589	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74HC589SA16.TR	SOP16	74HC589	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
AiP74HC589TA16.TR	TSSOP16	74HC589	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

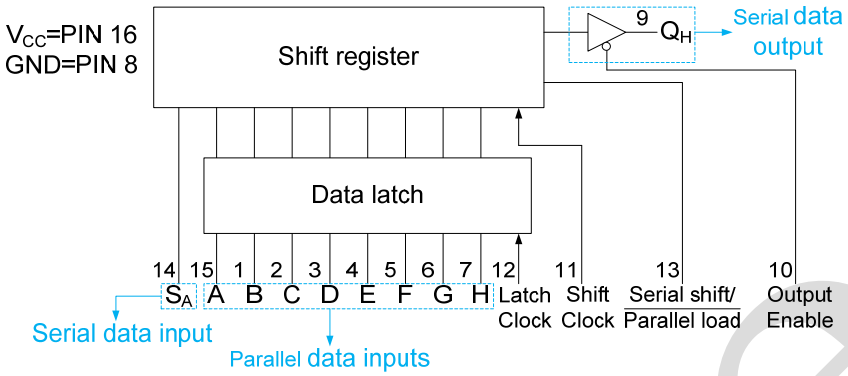
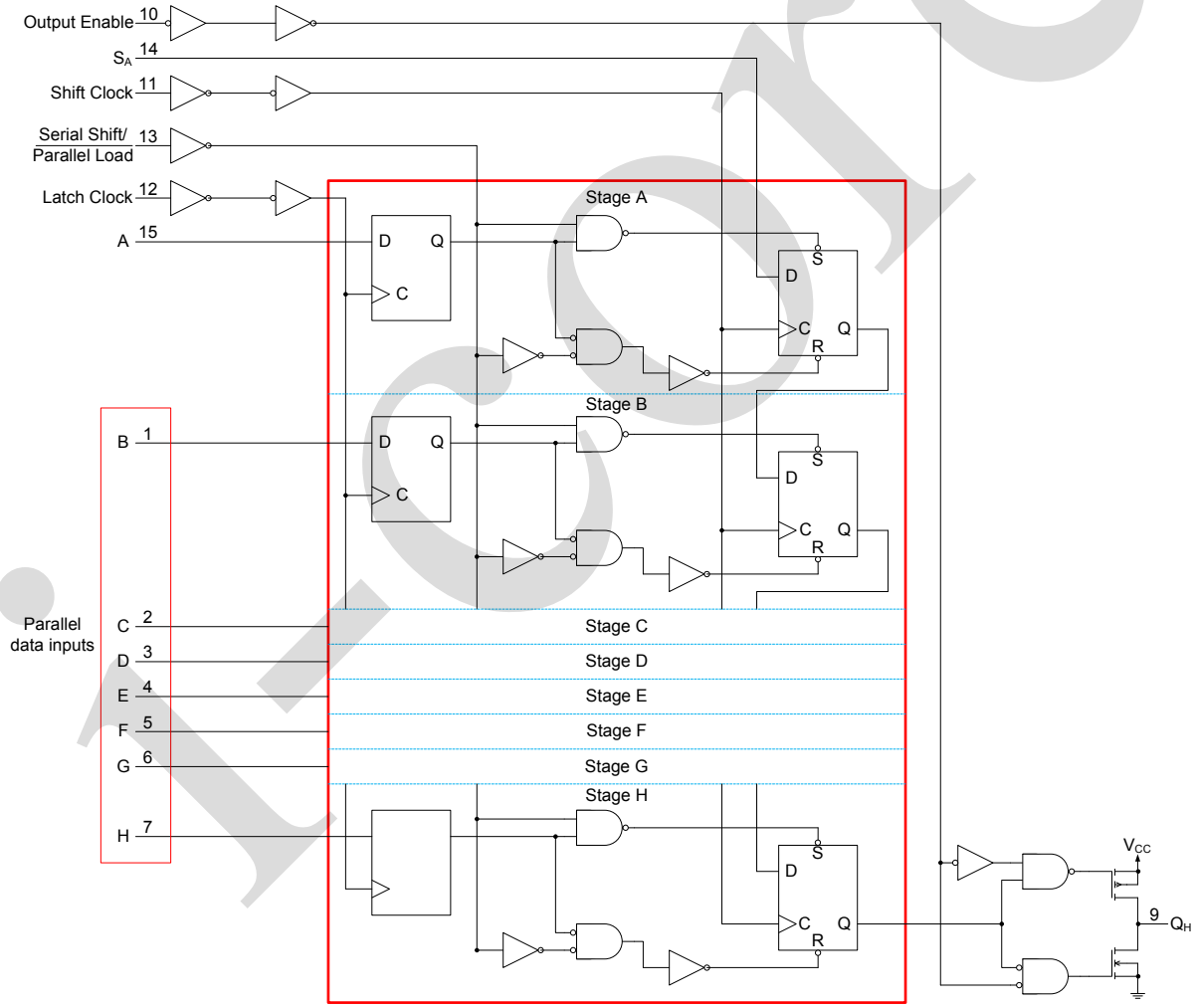


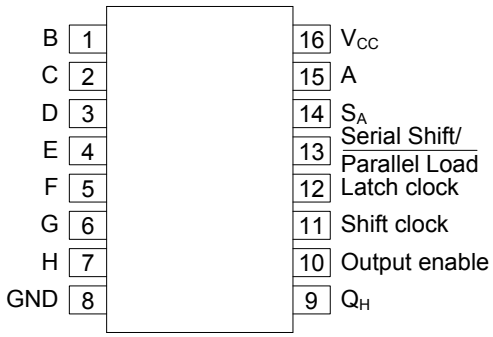
Figure 1. Logic diagram



*Stages C thru G (not shown in detail) are identical to stages A and B above.

Figure 2. Logic Detail

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	B	Parallel data input. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.
2	C	Parallel data input. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.
3	D	Parallel data input. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.
4	E	Parallel data input. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.
5	F	Parallel data input. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.
6	G	Parallel data input. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.
7	H	Parallel data input. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.
8	GND	ground (0V)
9	Q_H	Serial data output. This pin is the output from the last stage of the shift register. This is a 3−state output.
10	Output Enable	Active−low output enable A high level applied to this pin forces the Q_H output into the high impedance state. A low level enables the output. This control does not affect the state of the input latch or the shift register.
11	Shift Clock	Serial shift clock. A low−to−high transition on this input shifts data on the serial data input into the shift register and data in stage H is shifted out Q_H, being replaced by the data previously stored in stage G.
12	Latch Clock	Data latch clock. A low−to−high transition on this input loads the parallel data on inputs A−H into the data latch.
13	$\overline{\text{Serial Shift/ Parallel Load}}$	Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the data latch.
14	S_A	Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/ $\overline{\text{Parallel Load}}$ is high. Data on this input is ignored when Serial Shift/ $\overline{\text{Parallel Load}}$ is low.
15	A	Parallel data input. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.
16	V_{CC}	supply voltage

2.4、Function Table

Operation	Inputs						Resulting Function		
	Output Enable	Serial Shift/ Parallel Load	Latch Clock	Shift Clock	Serial Input S_A	Parallel Inputs A-H	Data Latch Contents	Shift Register Contents	Output Q_H
force output into high impedance state	H	X	X	X	X	X	X	X	Z
load parallel data into data latch	L	H	⎍	L, H, ⎍	X	a-h	a-h	U	U
transfer latch contents to shift register	L	L	L, H, ⎍	X	X	X	U	$LR_N \rightarrow SR_N$	LR_H
contents of Input latch and shift register are unchanged	L	H	L, H, ⎍	L, H, ⎍	X	X	U	U	U
load parallel data into data latch and shift register	L	L	⎍	X	X	a-h	a-h	a-h	h
shift serial data into shift register	L	H	X	⎍	D	X	*	$SR_A=D$, $SR_N \rightarrow SR_{N+1}$	$SR_G \rightarrow SR_H$
load parallel data in data latch and shift serial data into shift register	L	H	⎍	⎍	D	a-h	a-h	$SR_A=D$, $SR_N \rightarrow SR_{N+1}$	$SR_G \rightarrow SR_H$

Note:

LR=latch register contents

SR=shift register contents

a-h=data at parallel data inputs A-H

D=data (L, H) at serial data input SA

U=remains unchanged

X=don’t care

Z=high impedance

*=depends on Latch Clock input

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, All voltage referenced to GND, unless otherwise specified)

Characteristic	Symbol	Conditions		Value	Unit
supply voltage	V_{CC}	-		-0.5 to +7.0	V
input voltage	V_I	-		-0.5 to V_{CC}+0.5	V
output voltage	V_O	-		-0.5 to V_{CC}+0.5	V
input current	II	-		±20	mA
output current	IO	-		±35	mA
supply current	I_{CC}	-		±75	mA
ground current	I_{GND}	-		±75	mA
storage temperature	T_{stg}	-		-65 to +150	℃
Soldering Temperature	T_L	10s	DIP	245	℃
			SOP/TSSOP	260	℃

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.0	-	6.0	V
input/output voltage	$V_{I/O}$	-	0	-	V_{CC}	V
ambient temperature	T_{amb}	-	-40	-	+125	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=-40℃ to +85℃,, voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	V_{CC}	Conditions	Min	Typ.	Max.	Unit
minimum HIGH-level input voltage	V_{IH}	2.0V	-	1.5	-	-	V
		4.5V	-	3.15	-	-	V
		6.0V	-	4.2	-	-	V
maximum LOW-level input voltage	V_{IL}	2.0V	-	-	-	0.5	V
		4.5V	-	-	-	1.35	V
		6.0V	-	-	-	1.8	V
minimum HIGH-level output voltage	V_{OH}	2.0V	I_O=-20uA	1.9	-	-	V
		4.5V	I_O=-20uA	4.4	-	-	V
		6.0V	I_O=-20uA	5.9	-	-	V
		4.5V	I_O=-6.0mA	3.84	3.98		V
		6.0V	I_O=-7.8mA	5.34	5.48		V
maximum LOW-level output voltage	V_{OL}	2.0V	I_O=20uA	-	-	0.1	V
		4.5V	I_O=20uA	-	-	0.1	V
		6.0V	I_O=20uA	-	-	0.1	V
		4.5V	I_O=6.0mA	-	0.26	0.33	V
		6.0V	I_O=7.8mA	-	0.26	0.33	V
maximum input leakage current	I_I	6.0V	V_I=V_{CC} or GND,	-	-	±1.0	uA
maximum three-state leakage current	I_{OZ}	6.0V	V_I=V_{IL} or V_{IH}, V_O=V_{CC} or GND	-	-	±5.0	uA
maximum quiescent supply current	I_{CC}	6.0V	V_I=V_{CC} or GND, I_O=0uA,	-	-	40	uA

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	V_{CC}	Conditions	Min	Typ.	Max.	Unit
minimum HIGH-level input voltage	V_{IH}	2.0V	-	1.5	-	-	V
		4.5V	-	3.15	-	-	V
		6.0V	-	4.2	-	-	V
maximum LOW-level input voltage	V_{IL}	2.0V	-	-	-	0.5	V
		4.5V	-	-	-	1.35	V
		6.0V	-	-	-	1.8	V
minimum HIGH-level output voltage	V_{OH}	2.0V	I_O=-20uA	1.9	-	-	V
		4.5V	I_O=-20uA	4.4	-	-	V
		6.0V	I_O=-20uA	5.9	-	-	V
		4.5V	I_O=-6.0mA	3.70	-		V
		6.0V	I_O=-7.8mA	5.20	-		V
maximum LOW-level output voltage	V_{OL}	2.0V	I_O=20uA	-	-	0.1	V
		4.5V	I_O=20uA	-	-	0.1	V
		6.0V	I_O=20uA	-	-	0.1	V
		4.5V	I_O=6.0mA	-	-	0.40	V
		6.0V	I_O=7.8mA	-	-	0.40	V
maximum input leakage current	I_I	6.0V	V_I=V_{CC} or GND,	-	-	±1.0	uA
maximum three-state leakage current	I_{OZ}	6.0V	V_I=V_{IL} or V_{IH}, V_O=V_{CC} or GND	-	-	±10	uA
maximum quiescent supply current	I_{CC}	6.0V	V_I=V_{CC} or GND, I_O=0uA,	-	-	160	uA

3.3.3、AC Characteristics 1

(T_{amb}=-40℃ to +85℃, C_L=50pF, input t_r=t_f=6ns, unless otherwise specified)

Parameter	Symbol	Vcc	Conditions	MIN	TYP	MAX	Unit
maximum clock frequency (50% duty cycle)	f_{max}	2.0V	see Figure 3 and Figure 6	4.8	6	-	MHz
		4.5V		24	30	-	MHz
		6.0V		28	35	-	MHz
maximum propagation delay	t_{PLH}, t_{PHL}	2.0V	latch clock to Q_H, see Figure 3 and Figure 5	-	175	225	ns
		4.5V		-	40	50	ns
		6.0V		-	30	40	ns
maximum propagation delay	t_{PLH}, t_{PHL}	2.0V	shift clock to Q_H, see Figure 3 and Figure 6	-	160	200	ns
		4.5V		-	30	40	ns
		6.0V		-	25	30	ns
		2.0V	$\overline{\text{Serial Shift}}$/$\overline{\text{Parallel Load}}$ to Q_H, see Figure 3	-	160	200	ns
		4.5V		-	30	40	ns
		6.0V		-	25	30	ns
maximum propagation delay	t_{PLZ}, t_{PHZ}	2.0V	output enable to Q_H, see Figure 4 and Figure 7	-	150	170	ns
		4.5V		-	27	30	ns
		6.0V		-	23	25	ns
maximum propagation delay	t_{PZL}, t_{PZH}	2.0V	output enable to Q_H, see Figure 4 and Figure 7	-	150	170	ns
		4.5V		-	27	30	ns
		6.0V		-	23	25	ns
maximum output transition time	t_{TLH}, t_{THL}	2.0V	any output, see Figure 3 and Figure 5	-	60	75	ns
		4.5V		-	12	15	ns
		6.0V		-	10	13	ns
minimum setup time	t_{su}	2.0V	A-H to latch clock, see Figure 9	125	100	-	ns
		4.5V		25	20	-	ns
		6.0V		21	17	-	ns
		2.0V	serial data input S_A to shift clock, see Figure 10	125	100	-	ns
		4.5V		25	20	-	ns
		6.0V		21	17	-	ns
		2.0V	$\overline{\text{Serial Shift}}$/$\overline{\text{Parallel Load}}$ to shift clock, see	125	100	-	ns
		4.5V		25	20	-	ns
		6.0V		21	17	-	ns
minimum hold time	t_h	2.0V	latch clock to A-H, see Figure 9	30	25	-	ns
		4.5V		6	5	-	ns
		6.0V		6	5	-	ns
		2.0V	shift clock to serial data input S_A, see Figure 10	5	5	-	ns
		4.5V		5	5	-	ns
		6.0V		5	5	-	ns
minimum pulse width	t_W	2.0V	shift clock, see Figure 6	95	75	-	ns
		4.5V		19	15	-	ns
		6.0V		16	13	-	ns
		2.0V	latch clock, see Figure 5	100	80	-	ns
		4.5V		20	16	-	ns
		6.0V		17	14	-	ns
		2.0V	Serial Shift/	100	80	-	ns

		4.5V	$\overline{\text{Parallel Load}}$, see Figure 8	20	16	-	ns
		6.0V		17	14	-	ns
maximum input rise and fall time	t_r, t_f	2.0V	see Figure 5	-	-	1000	ns
		4.5V		-	-	500	ns
		6.0V		-	-	400	ns

3.3.4、AC Characteristics 2

(T_{amb}=-40℃ to +125℃, C_L=50pF, input t_r=t_f=6ns, unless otherwise specified)

Parameter	Symbol	Vcc	Conditions	MIN	TYP	MAX	Unit
maximum clock frequency (50% duty cycle)	f_{max}	2.0V	see Figure 3 and Figure 6	4	-	-	MHz
		4.5V		20	-	-	MHz
		6.0V		24	-	-	MHz
maximum propagation delay	t_{PLH}, t_{PHL}	2.0V	latch clock to Q_H, see Figure 3 and Figure 5	-	-	275	ns
		4.5V		-	-	60	ns
		6.0V		-	-	50	ns
maximum propagation delay	t_{PLH}, t_{PHL}	2.0V	shift clock to Q_H, see Figure 3 and Figure 6	-	-	240	ns
		4.5V		-	-	48	ns
		6.0V		-	-	40	ns
		2.0V	$\overline{\text{Serial Shift/Parallel Load}}$ to Q_H, see Figure 3	-	-	240	ns
		4.5V		-	-	48	ns
		6.0V		-	-	40	ns
maximum propagation delay	t_{PLZ}, t_{PHZ}	2.0V	output enable to Q_H, see Figure 4 and Figure 7	-	-	200	ns
		4.5V		-	-	40	ns
		6.0V		-	-	30	ns
maximum propagation delay	t_{PZL}, t_{PZH}	2.0V	output enable to Q_H, see Figure 4 and Figure 7	-	-	200	ns
		4.5V		-	-	40	ns
		6.0V		-	-	30	ns
maximum output transition time	t_{TLH}, t_{THL}	2.0V	any output, see Figure 3 and Figure 5	-	-	90	ns
		4.5V		-	-	18	ns
		6.0V		-	-	15	ns
minimum setup time	t_{su}	2.0V	A-H to latch clock, see Figure 9	150	-	-	ns
		4.5V		30	-	-	ns
		6.0V		26	-	-	ns
		2.0V	serial data input S_A to shift clock, see Figure 10	150	-	-	ns
		4.5V		30	-	-	ns
		6.0V		26	-	-	ns
		2.0V	$\overline{\text{Serial Shift/Parallel Load}}$ to shift clock, see	150	-	-	ns
		4.5V		30	-	-	ns
		6.0V		26	-	-	ns
minimum hold time	t_h	2.0V	latch clock to A-H, see Figure 9	40	-	-	ns
		4.5V		8	-	-	ns
		6.0V		7	-	-	ns
		2.0V	shift clock to serial data input S_A, see Figure 10	5	-	-	ns
		4.5V		5	-	-	ns
		6.0V		5	-	-	ns
minimum pulse width	t_W	2.0V	shift clock, see Figure 6	110	-	-	ns
		4.5V		23	-	-	ns
		6.0V		19	-	-	ns
		2.0V	latch clock, see Figure 5	120	-	-	ns
		4.5V		24	-	-	ns
		6.0V		20	-	-	ns
		2.0V	Serial Shift/	120	-	-	ns

		4.5V	$\overline{\text{Parallel Load}}$, see Figure 8	24	-	-	ns
		6.0V		20	-	-	ns

4、Testing Circuit

4.1、AC Testing Circuit

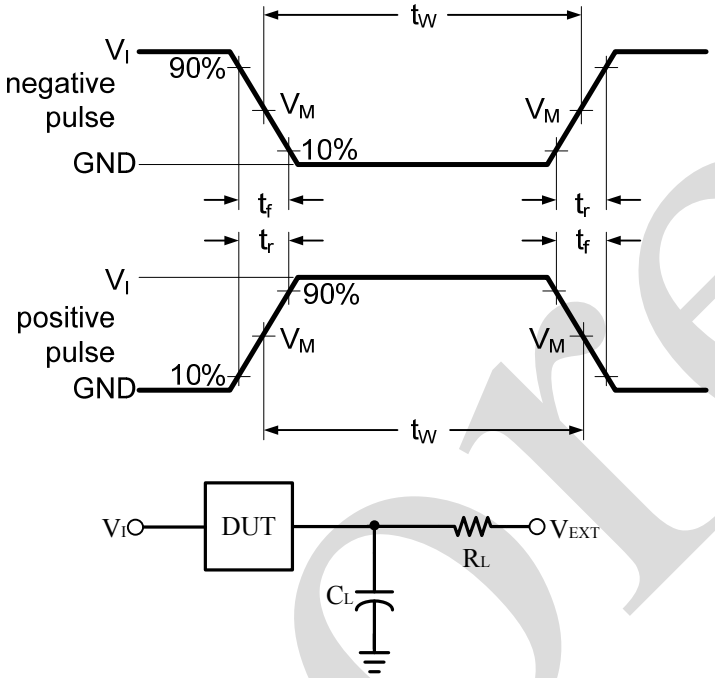


Figure 5. Test circuit for measuring switching times

C_L includes probe and jig capacitance.

4.2、Test Data

Type	Input		Load		V_{EXT}		
	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}/t_{PHL}	t_{PLZ}/t_{PZL}	t_{PHZ}/t_{PZH}
AiP74HC589	V_{CC}	3.0ns	50pF	1KΩ	Open	V_{CC}	GND

4.3、AC Testing Waveforms

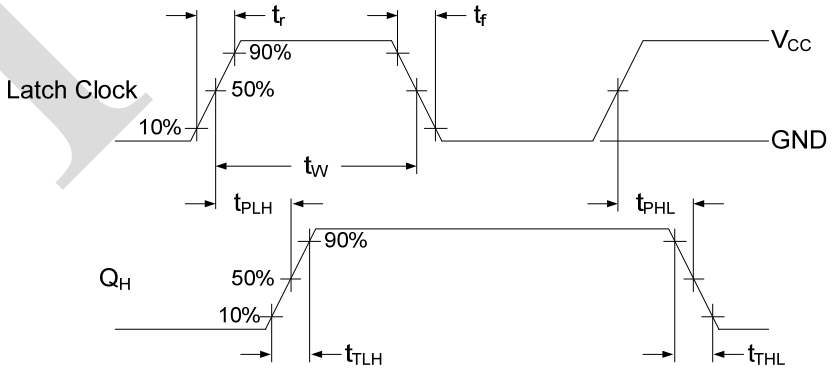


Figure 5 (Serial Shift/ $\overline{\text{Parallel Load}}$ =L)

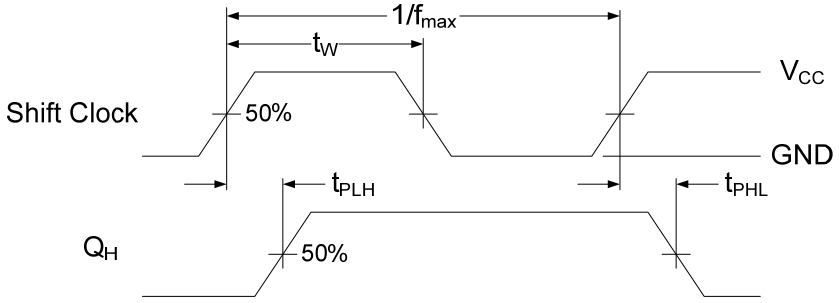


Figure 6 (Serial Shift/ $\overline{\text{Parallel Load}}$ =H)

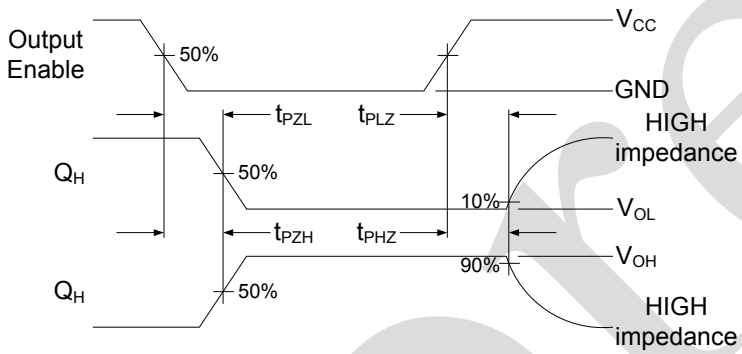


Figure 7

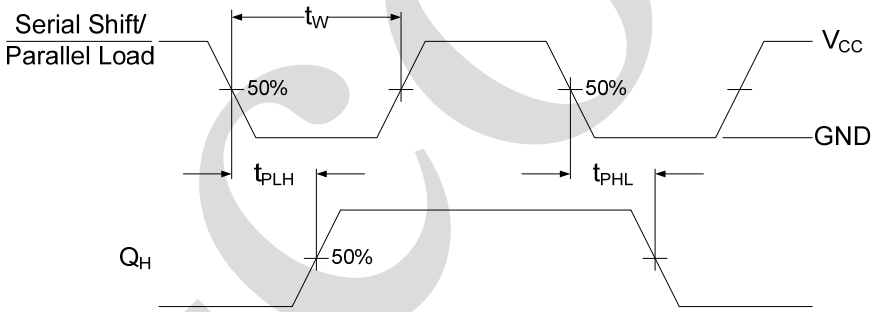


Figure 8

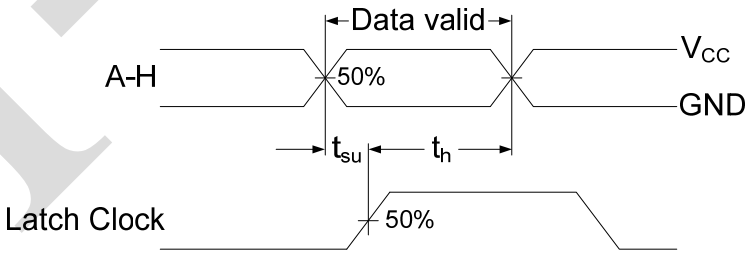


Figure 9

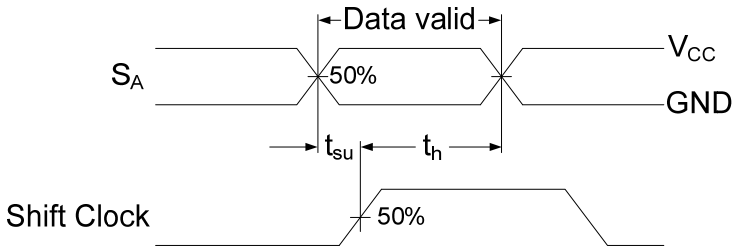


Figure 10

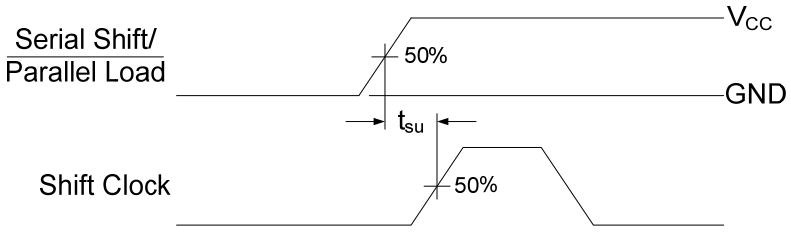


Figure 11

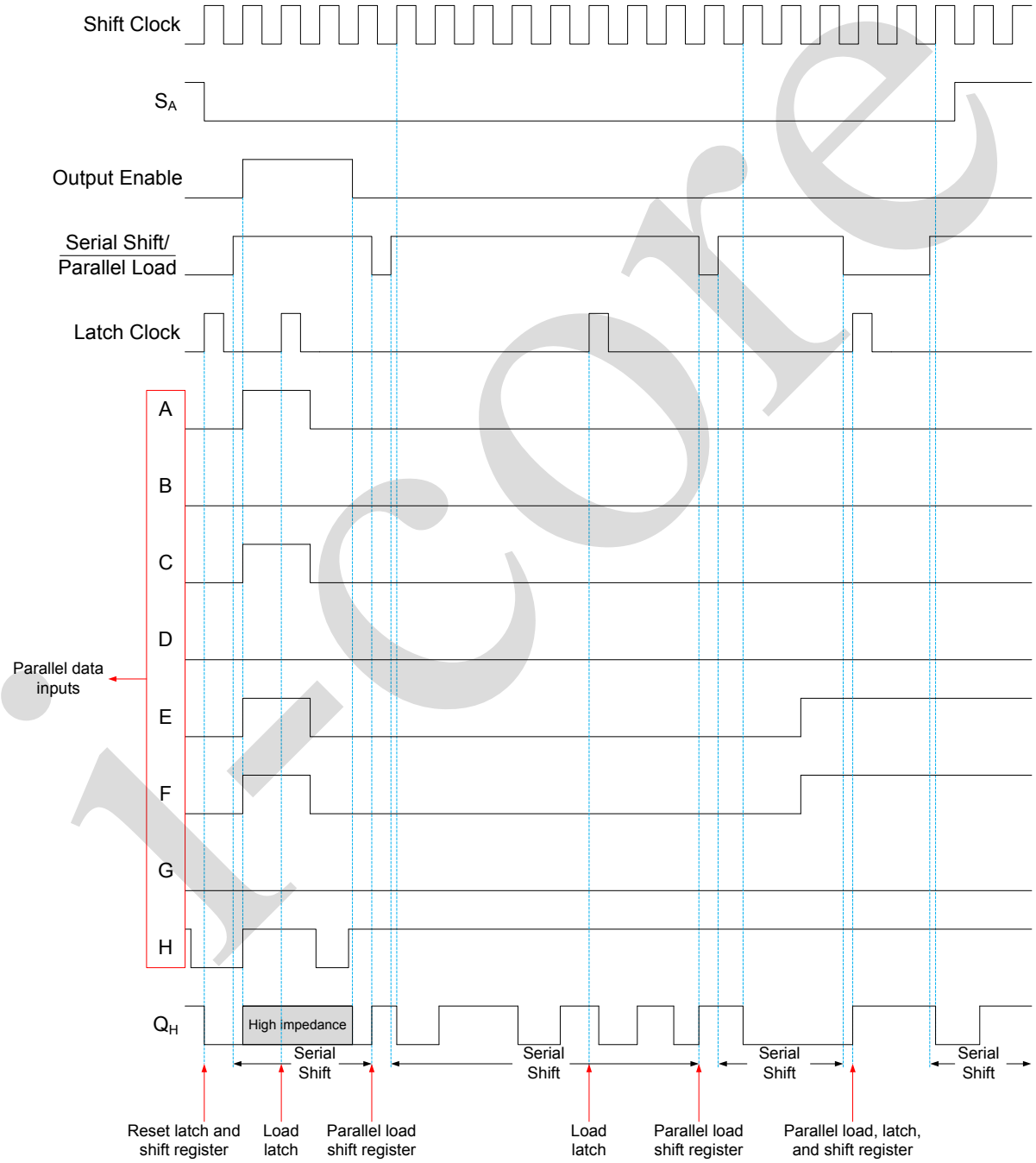
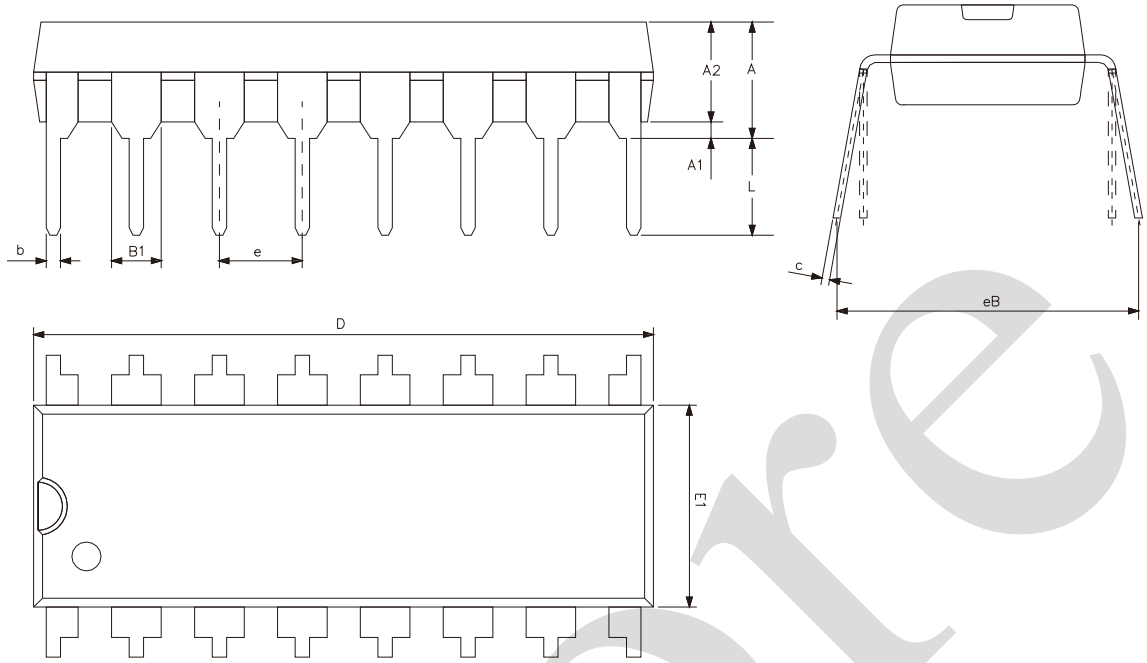


Figure 12. Timing Diagram

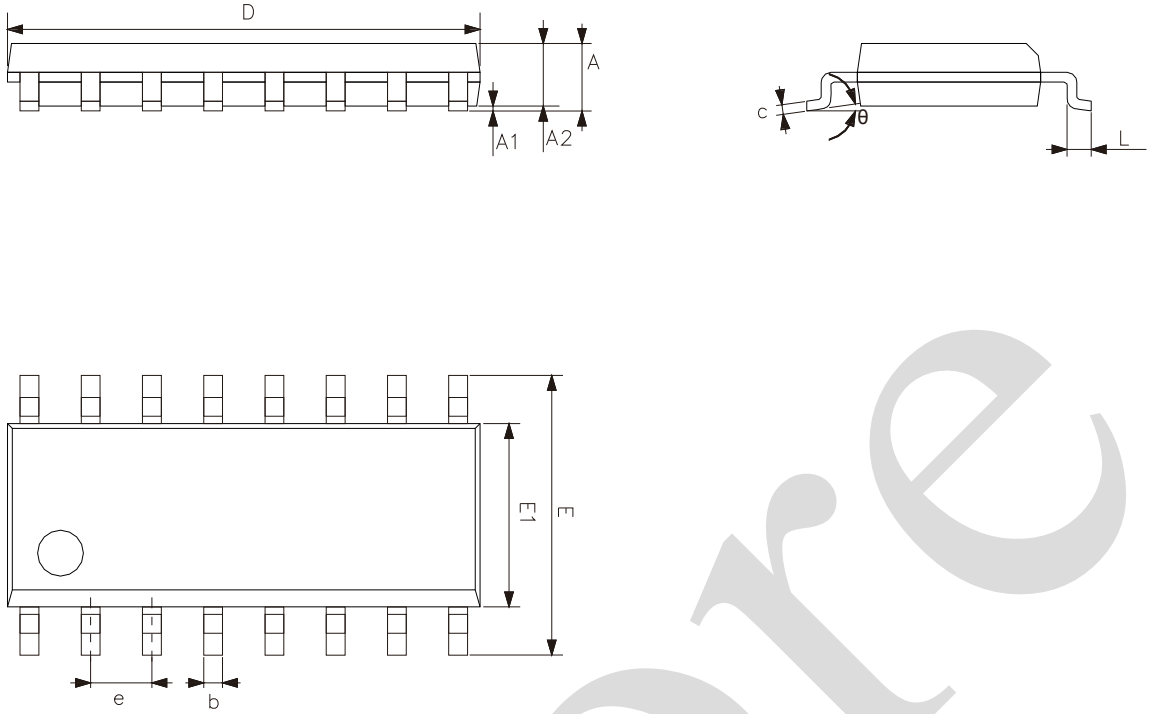
5、Package Information

5.1、DIP16



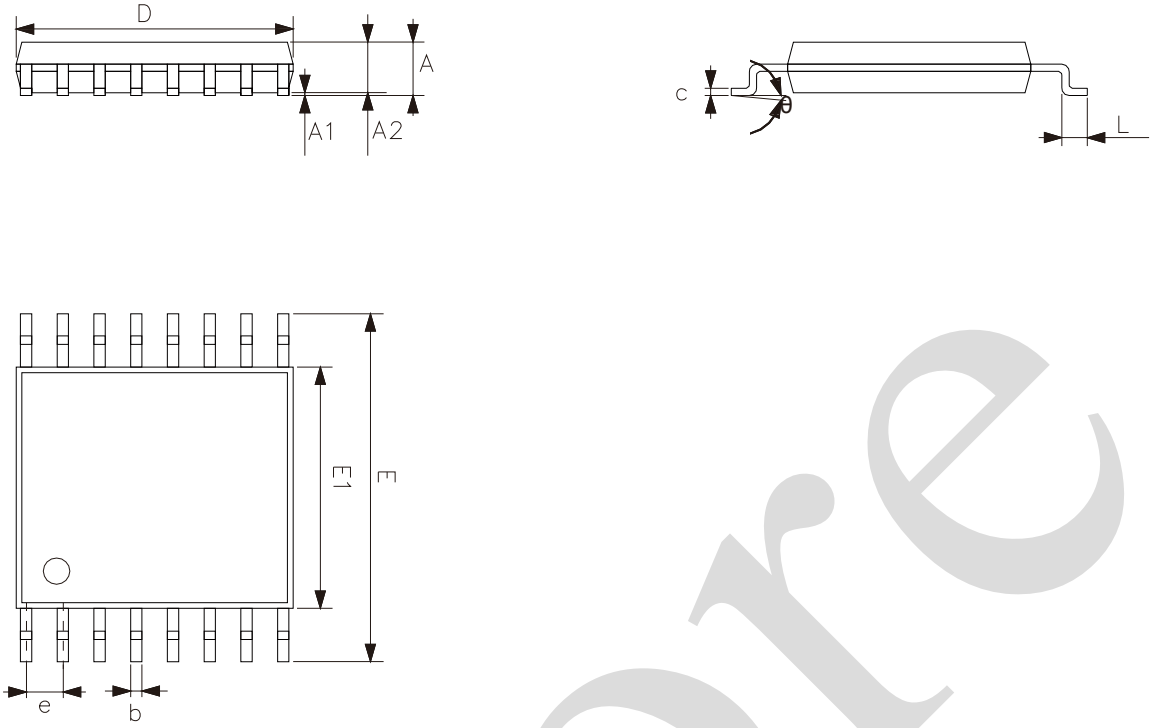
Symbol	Dimensions (mm)	
	Min.	Max.
A2	3.20	3.60
A1	0.51	-
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30

5.2、SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°

5.3、TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

We recommend you to read this chapter carefully before using this product.

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